

Hardware Design of a Tele-EEG Device For Detection of Neurophysiological Condition

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Abstract—The brain-machine interface systems bridge electrical engineering and neuroscience; developing new technologies helps better recognition of human's brain. The main idea of this research originates from the patients such that each patient with neural disorder should refer to a medical center to check his brain's health condition to sample his EEG signals and present the results to a specialist for further investigation. If this process can be done remotely by tele-medicine techniques, it will save cost and time. In tele-medicine method, the patient can record the EEG signal alone at home and send the results to his physician. To this end, this research employs Bluetooth to connect the interface system to the computer, and the patient can send the results to his physician after saving the data. Thus, the main purpose of designing this BCI system is to record EEG signals using a microcontroller and transmit them via Bluetooth to a computer and mobile phone such that the signal can be represented instantaneously in a GUI.

Keywords—Neural Interface, Tele-EEG, Neurophysiological Condition, Hardware Design.

I. INTRODUCTION

Many companies are currently working on designing and building human-machine interface systems, among which Neuralink [1] can be mentioned that has recently designed the initial version of the high-bandwidth brain implants, and its project is in the experimental phase. However, in this research, only one prefrontal cortex is targeted. The following scenario is considered in the design of this system:

First, the electrode is located on the region of interest on the head. This electrode receives the action potential of that point. Since this signal is weak, it is applied by an operational amplifier. Then, it is converted to a digital signal using an external ADC and transmitted to the microcontroller. The microcontroller transmits this data serially to the computer via Bluetooth to the computer or mobile phone. In the computer and mobile phone, a GUI is designed in which the signal is represented instantaneously. In this GUI, a digital filter can be applied, and the signaling duration can be changed. The important sections of this design are as follows:

- Designing a low-noise amplifier for the EEG signal
- PCB design
- Designing the digital filter in MATLAB to reduce the 50 Hz noise and eliminate artifacts of the signal
- Designing the graphic user interface

In the next part, the definition of basic concepts and general structure of the BCI system are described. Then, the conceptual design is presented.

A. Action Potential

The signals transmitted by the neurons are called the action potential. This action potential is generated as a result of ion exchange via neural cell membranes. To generate the action potential, first, the potential of the neural cell membrane is depolarized (getting more positive) until an overshoot is created. In Figure 1, this step is called the Rising Phase. After overshoot, the neural cell membrane is polarized again (getting more negative) until it achieves Rest. This step is also shown as the Falling phase in Figure 1, in which there is an undershoot before Rest. This procedure takes 5 to 10ms in most neural cells [2].

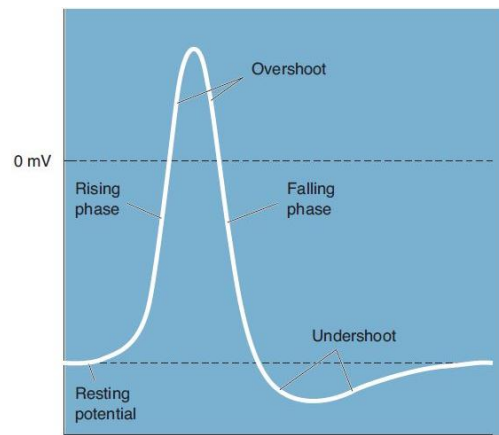


Figure 1. Different sections of the action potential [3]

B. Conventional Action Potential Measurement

The primary inter-membrane currents generate secondary ion currents along the cell membrane in the inner-cell and outer-cell spaces. The part of this current generated in the outer-cell space is directly responsible for generating the field potentials. The action potentials compared to post-synopsis potentials have a smaller field potential distribution (less penetration in the outer-cell environment) and shorter duration (about 1ms compared to the post-synopsis potentials that last about 15 to more than 200ms). Thus, the post-synopsis potentials accumulate in the cortex and propagate to the skull surface, and their resultant is recorded as EEG. The neurons that are usually responsible for generating EEG, their resultant fields can be measured, like pyramidal neurons of the cortex shown in Figure 2. Thus, the electrodes installed on the skull record the temporal and spatial resultant of the post-synopsis potentials of the membrane neurons and include slow and simultaneous potential changes in wide membrane areas that are generated by the pyramidal cells in parallel and orthogonal to the skull plane. The measurement of these electrodes is shown in Figure 2.

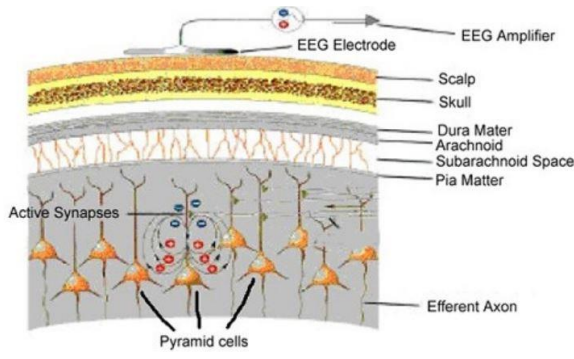


Figure 2. Measuring the action potential by the electrodes [4]

C. Conventional Action Potential Measurement

The amplitude of the signal measured by the electrode from the skull surface is about a few microvolts, such that its magnitude varies between 5 to 500 μV ; this weak signal should be amplified such that it can be measured. Also, 20 to 50 mV is generated by the skin and DC offset of the electrode. Therefore, an amplifier with high CMRR is required to eliminate the noise and DC offset of the common mode. Also, the frequency of the EEG signal is in the range of 1-40Hz that can be decomposed into four different frequency bands. Its summary is given in Table 1.

Table 1. Comparing different frequency bands of the EEG

Wave	Frequency	State	Lobe
α	7.5-13 Hz	Conscious Relaxed Eye open	Occipital Parietal Frontal
β	14-30 Hz	Anxious Alert Eye open	Frontal
θ	3.5-7.5 Hz	Sleep Small Children	Parietal Temporal
γ	< 3.5 Hz	Deep Sleep Small Children	

Figure 3 shows an example decomposing EEG signals into four frequency bands mentioned in Table 1.

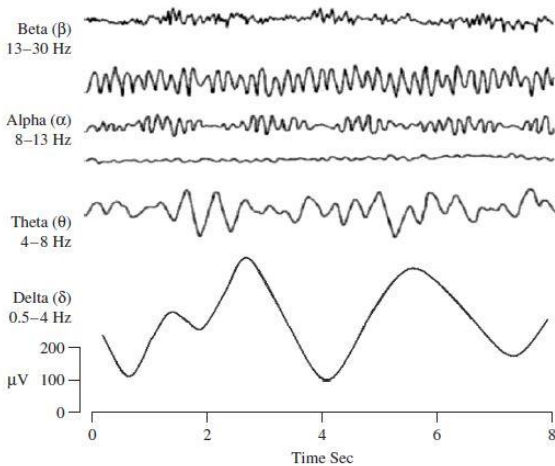


Figure 3. EEG signal decomposition [2]

In this project, the frequency band is considered because it can be received from an individual in complete consciousness and relaxation. Also, this frequency band is used due to the ease of measuring the signal from the front lobe. Therefore, other frequency bands should be filtered, which is discussed in chapter 4.

D. Conceptual Design

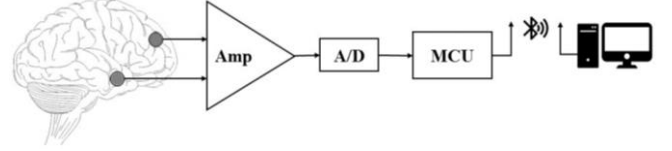


Figure 4. Conceptual model of the device

As shown in Figure 4, in the conceptual design of this device, only one channel is used to record EEG. The differential EEG signal of this channel is received by two electrodes that are located on the skull surface. But the signal amplitude is very low, about a few microvolts, which should be amplified. To this end, in the next block, an amplifier is used that amplifies the signal considering its gain so that the subsequent blocks can measure the signal. In the next block, the analog signal is converted into binary data using an external A/D converter. An external A/D is used to achieve a higher resolution, and the analog signal is converted to a binary signal with a higher sampling rate. Then, the digital signal enters the microcontroller, and it is buffered. The USART communication protocol should also be activated simultaneously to transmit the buffered binary data to the computer or mobile phone via Bluetooth. The received signal is read by the GUI and represented after applying the desired filters.

In the next parts, the hardware facilities required to achieve the final design are given. Then, the interface is designed, and its software is introduced. After that, signal processing is described. Finally, the results and observations are given. Also, an appendix are given at the end of this report, including all schematics, and PCB of the system.

II. HARDWARE DESIGN

A. Amplifier

To amplify the physiological signals, Instrument Amplifier is used. The most well-known op-amp in this context is the AD620 IC, which is shown in Figure 5.

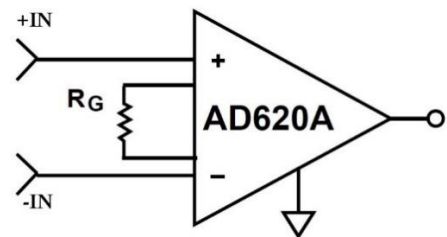


Figure 5. AD620 IC

The resistance R_G is used to adjust the gain of this IC. Also, considering the datasheet of this IC, the gain is obtained using Eq. (1):

$$(1) \quad Gain = 1 + \frac{49.4 \text{ k}}{R_G}$$

Now, to design considering the desired amplitude, R_G is determined using the following equation:

$$EEG \text{ Amplitude: } 5 \text{ to } 500 \mu V$$

We want to obtain a maximum of 5v at the output that can be sensed by the ADC, therefore:

$$Gain = \frac{5}{500 \mu V} = 10000$$

Considering Eq. (1), we have:

$$10000 = \frac{49.4 \text{ k}}{R_G}$$

$$R_G = 4.94 \Omega$$

The closest standard resistance to this value is 4.84Ω . Considering Eq. (1), the gain is obtained for resistance of 10144; if a 500uV input is applied, the signal obtained at the output would be:

$$\text{Maximum Output} = 500 \mu V \times 10144 = 5.072 \text{ volt}$$

In other words, if we want to determine a reference voltage in the next stage in which the ADC IC is located, the maximum reference voltage would be 5.02V. Also, the AD620 IC operates linearly in the following output swing:

$$\text{Output Swing} = -V_{SS} + 1.1 \text{ volt to } +V_{SS} - 1.1 \text{ volt}$$

This IC requires symmetric voltages for supply. Therefore, if -12 to +12 volt are used for supply, the output swing would be as follows:

$$\begin{aligned} \text{Output Swing} &= -12 + 1.1 \text{ volt to } +12 - 1.1 \text{ volt} \\ &= +10.9 \text{ volt to } -10.9 \text{ volt} \end{aligned}$$

The summary of the designed amplifier is given in Table 2.

Table 2. Characteristics of the Amplifier stage

$R_G(\Omega)$	Gain	Max Out (v)	Swing (v)
4.84Ω	10144	5.072	-10.9 to +10.9

B. Analog to Digital Converter (A/D)

To increase the accuracy of this system, an external ADC called MCP3201 is used, which is a 12-bit IC with a 5v supply and 100kps sampling rate. This IC is connected to the microcontroller via the SPI protocol. The Block diagram of this ADC is shown in Figure 6. Considering Figure 6, the output binary data is on the DOUT pin that should be connected to the MISO pin of the microcontroller.

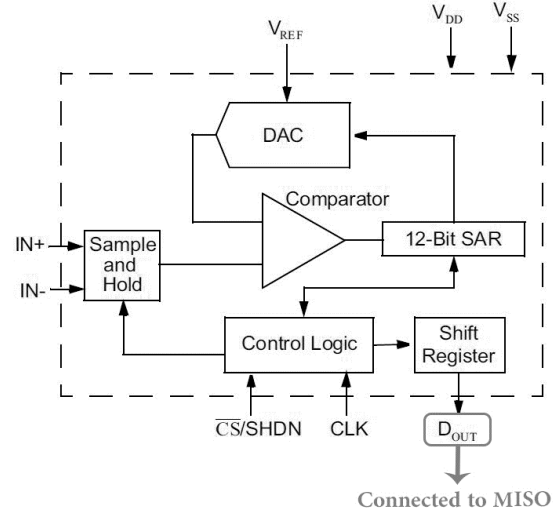


Figure 6. Functional block diagram of MCP3201

Since the resolution of this ADC is 12 bits, the reference voltage of 4.096v is used to achieve an integer accuracy.

$$Accuracy = \frac{V_{ref}}{2^{Resolution}} = \frac{4.094}{2^{12}} = 1 \text{ mV}$$

In this design, the output of LM4040-4.1 IC is used as the reference voltage of the ADC. As mentioned, this IC is connected to the microcontroller via the SPI protocol. In this mode, the IC operates with a 250kHz clock, and the sampling data is buffered as 8-bit data in the SPDR register. Figure 7 shows the settings of the SPI in this mode.

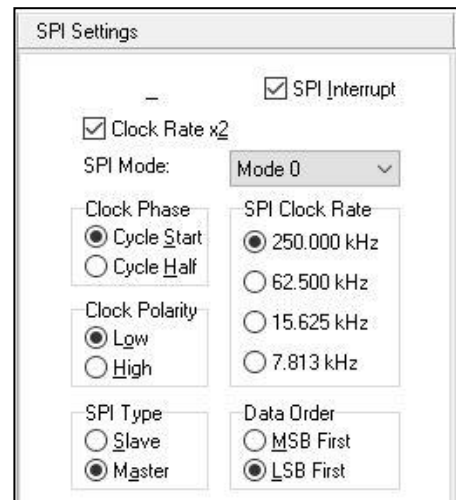


Figure 7. SPI settings in the code wizard

C. Serial Communication

HC05 Bluetooth module is used to connected the microcontroller with the computer. This connection is carried out via the USART protocol that its TX should be activated in the microcontroller. The default Baud rate is 9600 in double-speed mode. Also, even parity and a stop bit are used.

D. Power Supply

The general supply of this system is $+12v$, but other sections require a $+5v$ supply. A 7805 regulator provides this supply. Also, IC 555 is used to generate the voltage of $-12v$ required by the AD620 Op-amp. The circuit is simulated in Proteus, as shown in Figure 8.

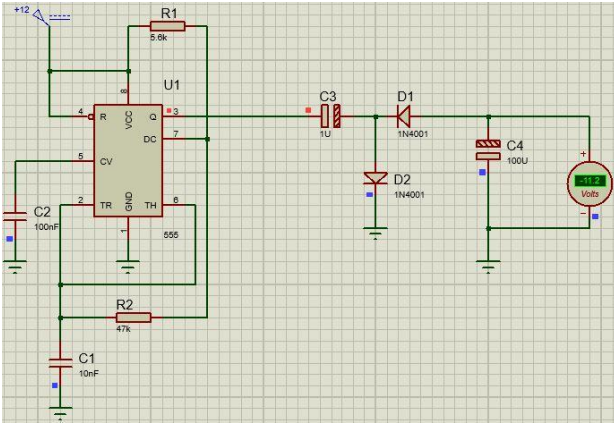


Figure 8. Simulation of -12 volt generated by IC 555

III. SOFTWARE AND UI DESIGN

MATLAB is used in the GUI design section, and a user interface is designed. It is only sufficient to recall the TeleEEG function in MATLAB so that a GUI like the one in Figure 9 is opened. The Baud rate required to call the COM port is 9600 by default.

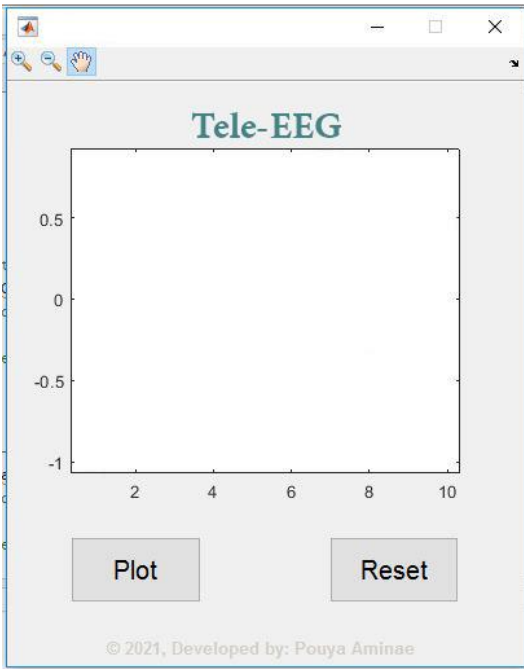


Figure 9. GUI

Figure 10 illustrates a mobile application that is developed for android users. In the application, notch filter and EMG filter have been considered to reduce the effect of 50 Hz noise and also unwanted artifacts. Mental status can be shown as Normal or Abnormal based on trained ML models. We will discuss our algorithm for the prediction of neural conditions in future papers.

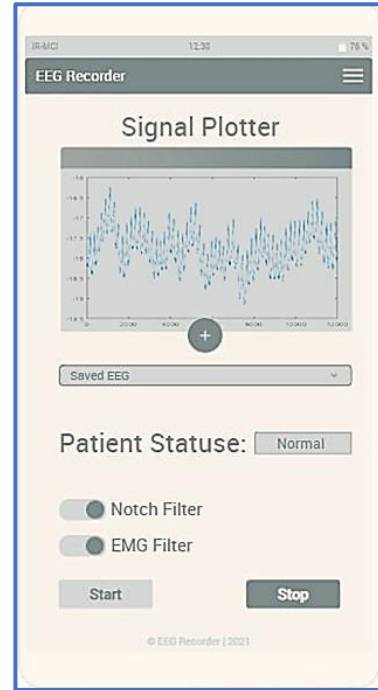


Figure 10. Mobile Application

IV. SIGNAL PROCESSING

Since the 50Hz noise affects any electronic device, it should be filtered first. So, a notch filter with a cut-off frequency of 50Hz should be designed. To this end, the Filter Designer toolbox of MATLAB is used, and the most optimal notch filter is selected, which is of 4th order and 2nd Chebyshev type. The code of this filter is given in the appendix. The frequency response of this filter is shown in Figure 11.

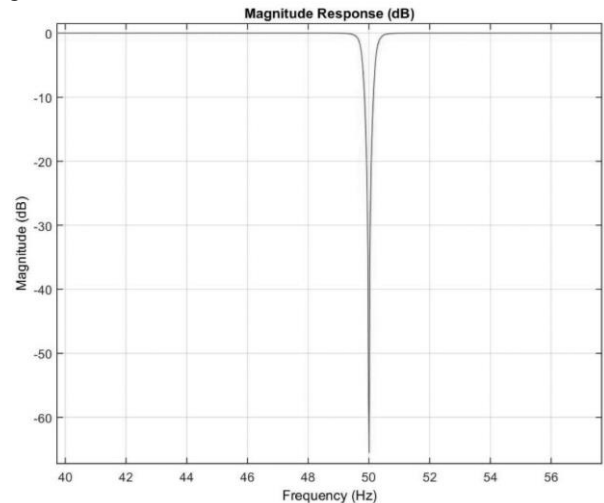
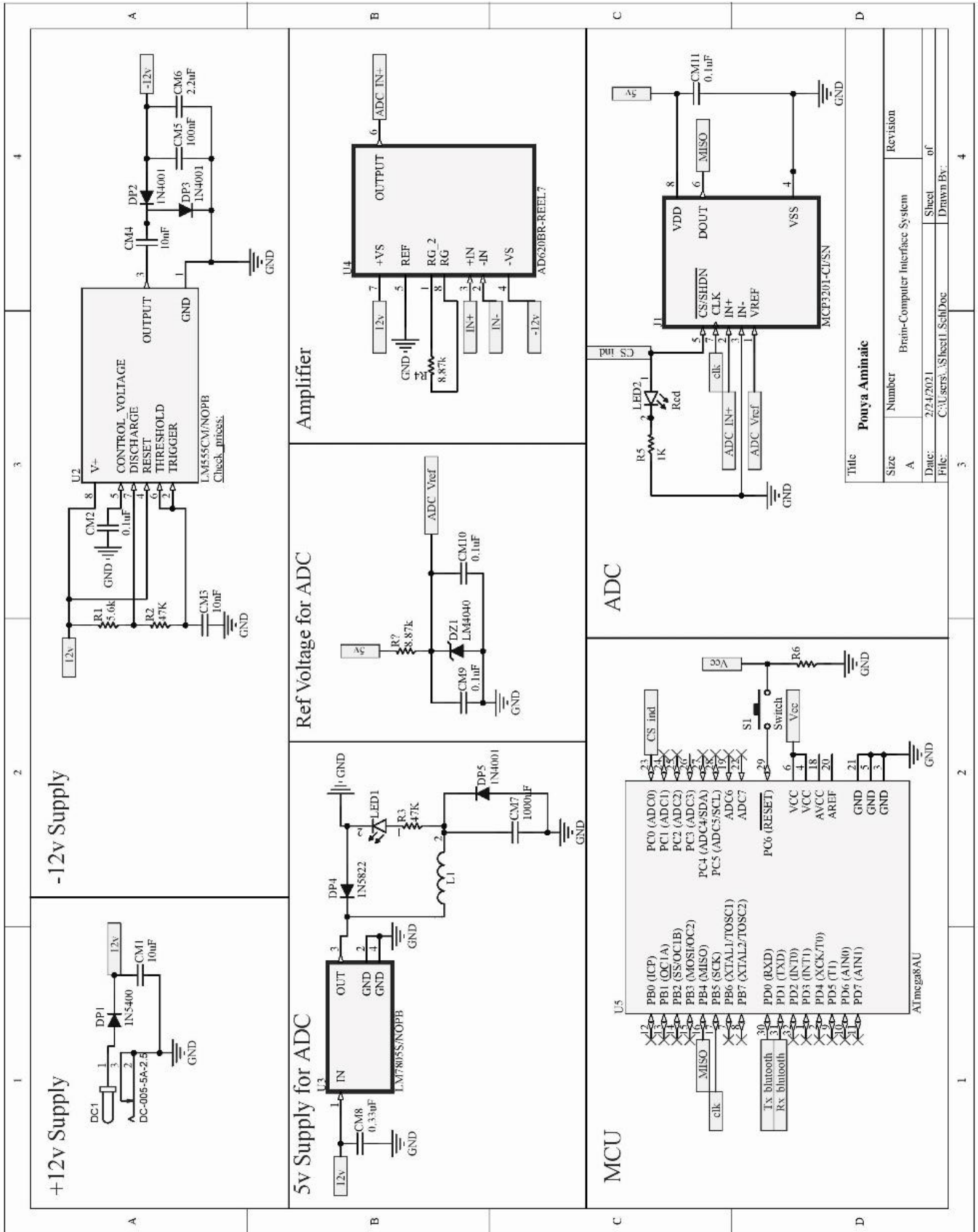


Figure 11. The magnitude of the filter's frequency response

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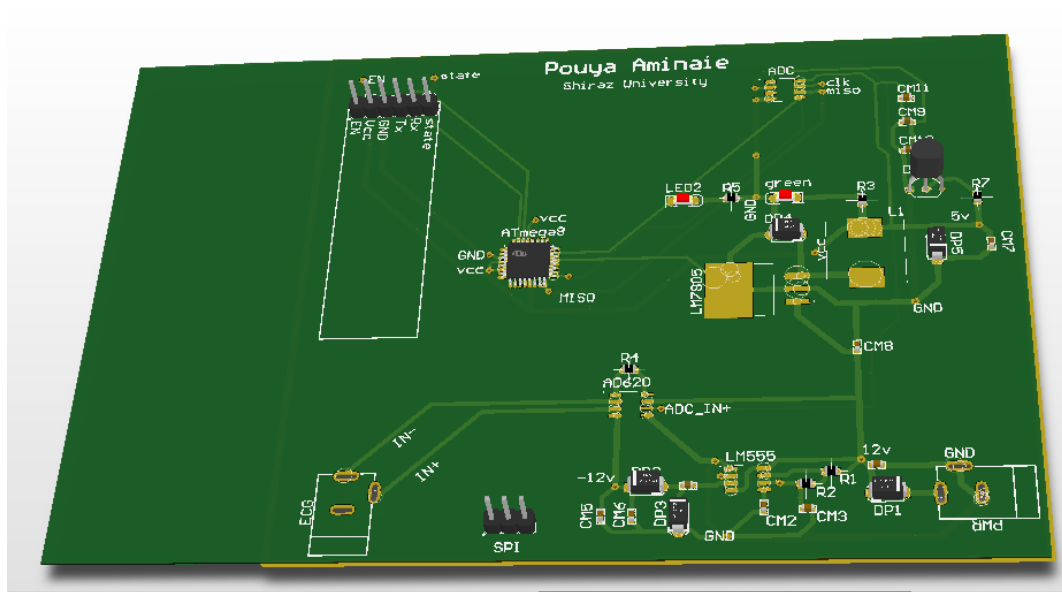
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The schematic designed in Altium

APENDIX II: PCB

A. Top Layer



B. Bottom Layer

