Supporting Information

Photocurrent Switching of Monolayer MoS_2 using Metal–Insulator Transition

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1. Growth conditions for MoS_2

In order to synthesize MoS_2, a promoter for the growth seed was first prepared by dissolving sodium cholate (SC) hydrate (Sigma-Aldrich, C6445) into DI water (0.1 g of SC in 10 ml of DI water). We also separately prepared ammonium molybdate tetrahydrate (11.5 mM, Sigma-aldrich, 431346) as a Mo precursor, and mixed it with the promoter. A droplet of the mixture solution was dropped onto a SiO_2/Si wafer and spin-casted at 2800 rpm for 1 min. A total of 150 mg of sulfur chip on the substrate was placed in the growth system with two separate heating zones. The preheating zone temperature was increased to 210 ºC at a rate of 42 ºC/min for the sublimation of S. The growth zone was heated to 780 ºC. The entire process was carried out under 500 sccm N_2 for 16 min. The as-grown monolayer MoS_2 flakes are shown in Fig. S1(a). The length of each side of the triangular MoS_2 flake (indicated by an

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arrow) is approximately 50 μm. To confirm the crystallinity, the flakes were studied via Raman spectroscopy using laser light with a wavelength of 532 nm. Spectroscopy reveals fingerprint-like peaks of E^1_{2g} and A_{1g} at 383.1 cm^{-1} and 402.5 cm^{-1}, respectively. The peak separation between E^1_{2g} and A_{1g} is used to signify the monolayer of MoS_2. In Fig. S1(b), the peak separation is approximately 19.4 cm^{-1}, which is consistent with the monolayer.

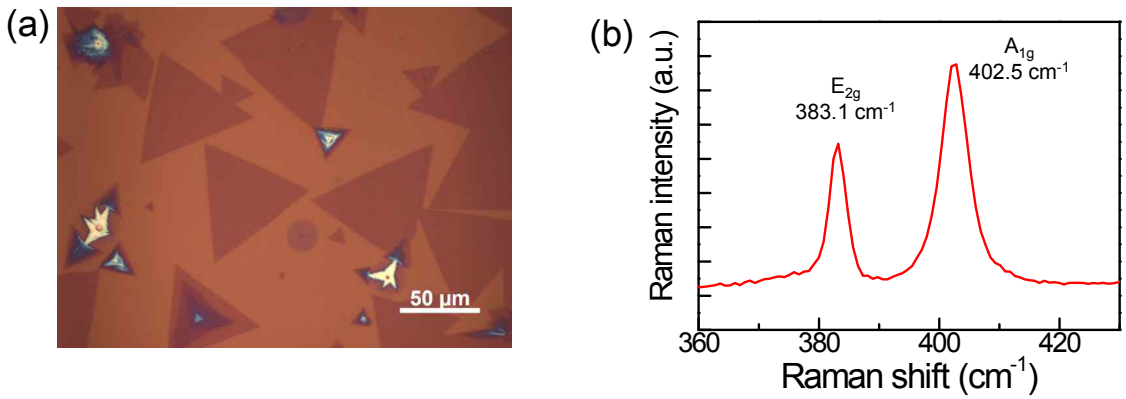

Figure S1. (a) Optical image and (b) Raman spectroscopy of CVD-grown MoS_2 mon olayer flakes.

2. Carrier concentration of MoS_2 in parallel capacitor model

We can obtain the carrier concentration of MoS_2 induced by the gate bias by using a parallel capacitor model. By drawing a linear tangential line (red line) in the electric transport graph (black line) at V_{gs} giving the transconductance peak, the threshold voltage (V_{th} ~ 19 V) is extracted. At the onset of the threshold voltage point, the channel changes from nonconducting to conducting, and the number of electrons in the channel increases. This increase in the number of induced electrons n_g caused by the gate bias can be calculated using a parallel capacitor model (eq. 1).

$$n_g = \frac{C_{ox}(V_{gs} - V_{th})}{q} \text{(eq. 1)}$$

where q is the electric charge of an electron, and C_{ox} is the capacitance of the gate oxide. In our samples, 300-nm-thick silicon oxide is used as the gate oxide (the dielectric constant is 3.9). Using these parameters, the number of induced electrons is indicated by the blue line. From our calculations near V_{gs} = 60 V, the carrier concentration reaches approximately n = $1.0 \times 10^{13}/cm^2$.

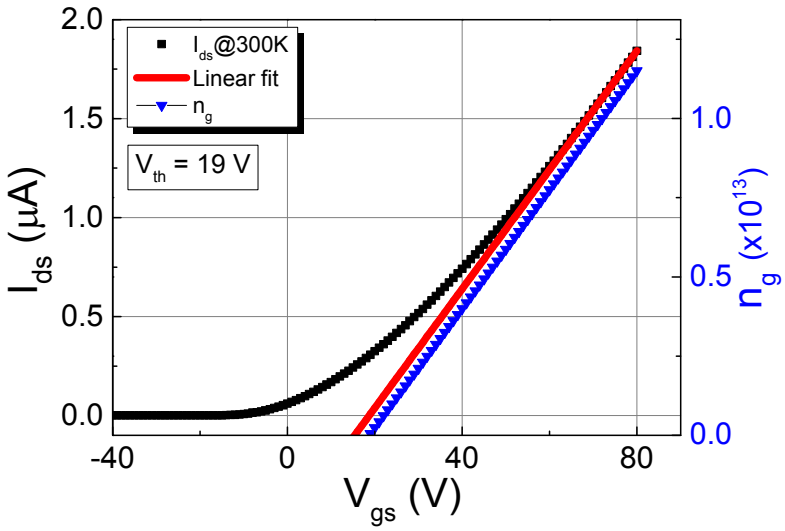

Figure S2. Drain current I_{ds} (Y1 axis) and channel carrier density n_g (Y2 axis) as fun ctions of backgate bias V_{gs}.

3. Extraction of SBH of MoS_2 FET

We now characterize the SBH of our devices. MoS_2 FETs on SiO_2 and h-BN substrates are fabricated with four electrodes, as shown in Figs. S3(a) and 3(b). The fabrication of a four-electrode device is intended to probe the series resistance or channel resistance in order to evaluate an accurate SBH. Thus, we study the total resistance (R_{total}), contact resistance

($R_{contact}$), and channel resistance ($R_{channel}$) of our devices. $R_{channel}$ is obtained by running current between electrodes 1 and 4 and measuring the voltage between electrodes 2 and 3 in Fig. S3(a) [1]. The resistance between electrodes 2 and 3 measured with two probes gives R_{total} of the device. Then, $R_{contact}$ is extracted by subtracting $R_{channel}$ from R_{total}. These three different types of device resistance on the SiO_2 substrate are plotted as a function of $V_{gs} > V_{th}$, as shown in Fig. S5(a). V_{ds} of the device on the SiO_2 substrate is 0.3 V. $R_{contact}$ is always larger than $R_{channel}$. The gap between $R_{contact}$ and $R_{channel}$ grows larger as V_{gs} increases.

The same comparative study is carried out using h-BN as a substrate. Remarkably, a MoS_2 FET on an h-BN substrate has $R_{contact}$ that is much larger than $R_{channel}$, as shown in Fig. S5(c). In addition, $R_{channel}$ of a MoS_2 FET on h-BN substrate is much lower than that on SiO_2. It is expected that the lower $R_{channel}$ for h-BN substrates results from a reduced scattering of carriers by ionic impurities that populate less on h-BN than SiO_2 substrates. It is possible that the inner metal contacts from van der Pauw method can perturb the electronic structure. In order to avoid such an artifact from the measurement, transfer line [2,3] or Hall bar measurement [4,5] is recommended.

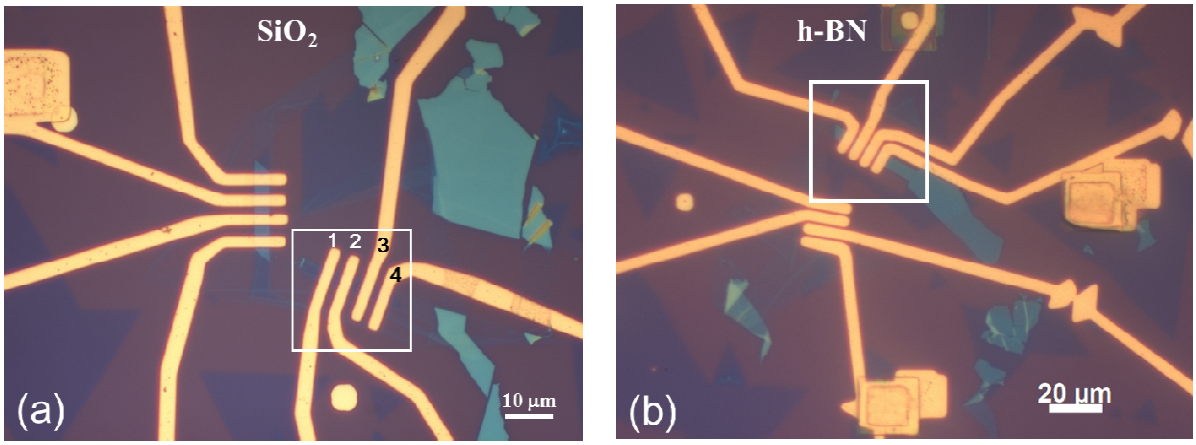

Figure S3. Optical images of four-electrode MoS_2 devices on (a) SiO_2 substrate and (b) h-BN layer.

In order to compare the SBHs for different substrates, devices are characterized by sweeping V_{ds} (-1.0 to 1.0 V) and V_{gs} (0 to 50 V), as shown in the insets of Figs. S4(a) and 4(b). The temperature of the device changes from 300 to 80 K in decrements of 20 K. Prior to the estimation of the SBH, ideality factor *n*, which measures the deviation from thermionic emissions by considering the effect of traps, is calculated. For *n*, the thermionic I-V relationship of a Schottky barrier is given as $I_{ds} = I_s e^{qV/n\kappa_B T}(1 - e^{-qV/\kappa_B T})$, where I_s is the saturation current, which can be further expressed as $I_s = AA^* T^2 e^{-q\phi_B/\kappa_B T}$, where A is the junction area and A* is the Richardson constant [6]. The slope of $\ln\left[\frac{I_{ds}}{1 - e^{-qV/\kappa_B T}}\right]$ vs. $V_{contact}$ is equal to $\frac{q}{n\kappa_B T}$. Using this, we estimated the value of *n* for our device. $V_{contact}$ is shown in Figs. S4(a) and 4(b) for both devices.

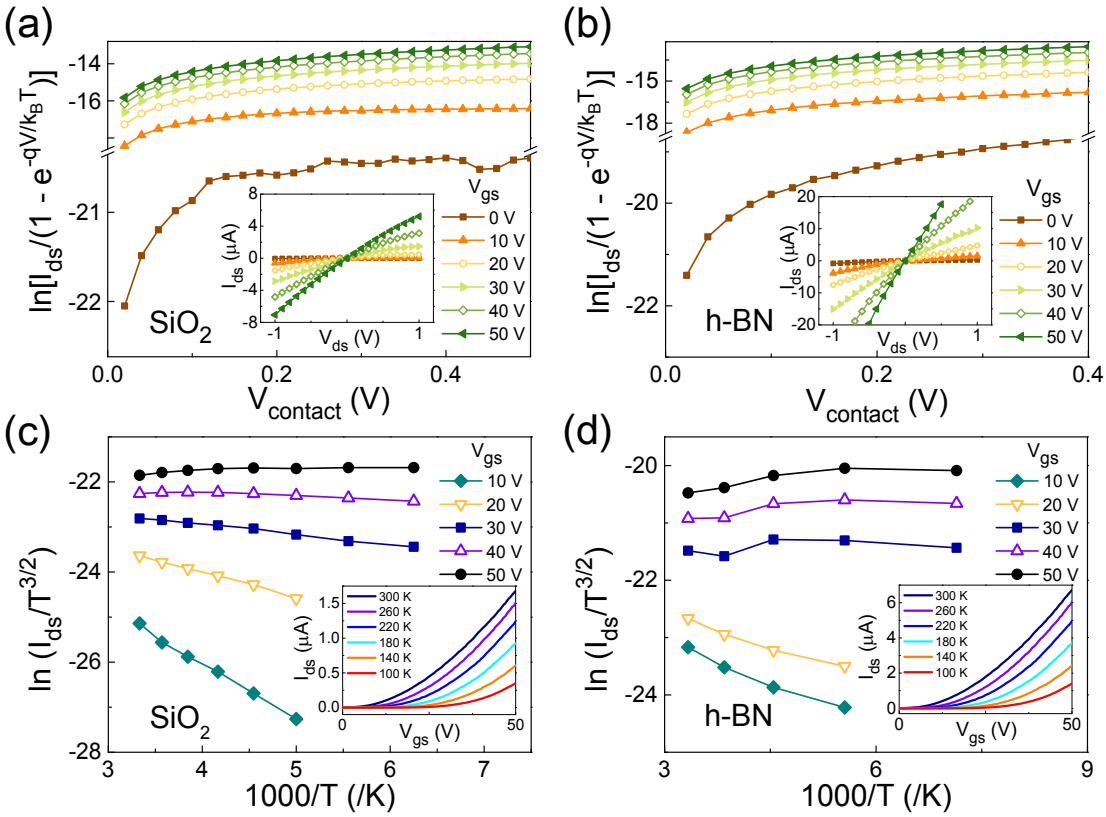

Figure S4. $\ln\left[\frac{I_{ds}}{1-e^{-qV/\kappa_B T}}\right]$ vs. $V_{contact}$ at various V_{gs} of MoS_2 FET on (a) SiO_2 and (b) h-BN substrates. The inset shows I_{ds}-V_{ds} curves at various V_{gs} on the former and the latter. Richardson plots at different V_{gs} of MoS_2 FET on (c) SiO_2 and (d) h-BN substrate. The inset shows I_{ds}-V_{gs} curves at various temperatures on the former and the latter.

A comparison of *n* for two- and four-terminal devices exhibits the same value of 2.3 for the SiO_2 substrate. Using the same process for the h-BN device, we obtained a slightly lower ideality factor (n = 1.9) compared with that of SiO_2 gate dielectrics. A higher ideality factor for SiO_2 compared with h-BN results from the increased effect of trap sites in the channel in SiO_2.

The SBH of MoS_2 FETs on SiO_2 and h-BN substrates is estimated using an I-T relation shown in inset of Figs. S4(c) and 4(d), also known as the *Richardson plot*:

$\ln(\frac{I_{ds}}{T^{3/2}}) = \ln(AA^*) - q(\phi_B - V/n)/\kappa_B T$ shown in Figs. S4(c) and 4(d). At a given V_{ds}, from the slope of $\ln(\frac{I_{ds}}{T^{3/2}})$ vs. 1000/T, we calculate the Schottky barrier height. When V_{ds} = 0.3 V, SBH depending on V_{gs}-V_{th} is plotted in Fig. S5(b) for the device on a SiO_2 dielectric. The SBH near the flat band voltage ranges roughly from 165 to 135 meV, and no remarkable difference in SBH is observed with or without series resistance. This implies that $R_{contact}$ is much more dominant over $R_{channel}$ near the flat band voltage. The SBH of the device on an h-BN layer is found to be much lower (ranging approximately from 70 to 60 meV) than that of the device on SiO_2. Again, the difference of the SBH in the two- and four-electrode measurements is approximately 10 meV. Thus, the effect of $R_{channel}$ becomes more significant compared with that of the device on SiO_2. This is a result of a lower SBH for the MoS_2 FET on an h-BN layer. From Figs. S5(b) and 5(d), it is confirmed again that the SBH is much lower on h-BN than on SiO_2 substrate.

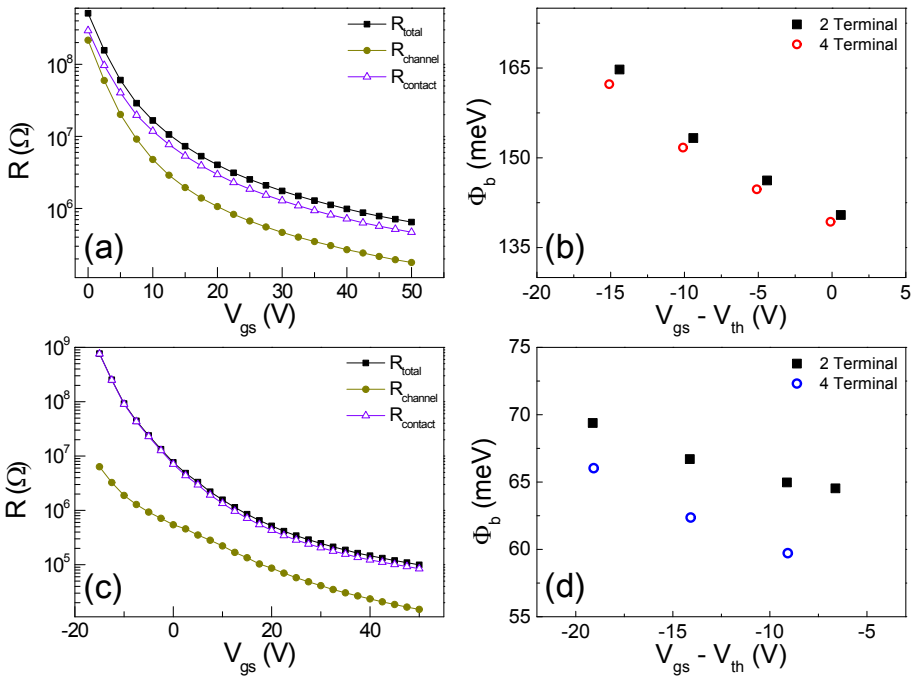

Figure S5. (a) R_{total}, $R_{channel}$, and $R_{contact}$ and (b) SBH of MoS_2 device on SiO_2 substrate. (c) R_{total}, $R_{channel}$, and $R_{contact}$ and (d) SBH of MoS_2 device on h-BN substrate.

4. Experimental setup

To better understand the photocurrent mechanism in our sample, we utilized a custom-made photocurrent scanning system, as shown in Fig. S6(a). The scanning system has a CW laser with a wavelength of 532 nm and an objective lens with a numerical aperture of 0.60. Using a mirror scanning system, the laser light was rastered on the surface of the sample [inset of Fig. S6(a)], which was located inside a mini-cryostat. The scanning area was approximately 80 × 80 μm^2. In order to characterize the samples, we employed DC and AC photocurrent measurement systems whose schematics are shown in Figs. S6(b) and S6(c), respectively.

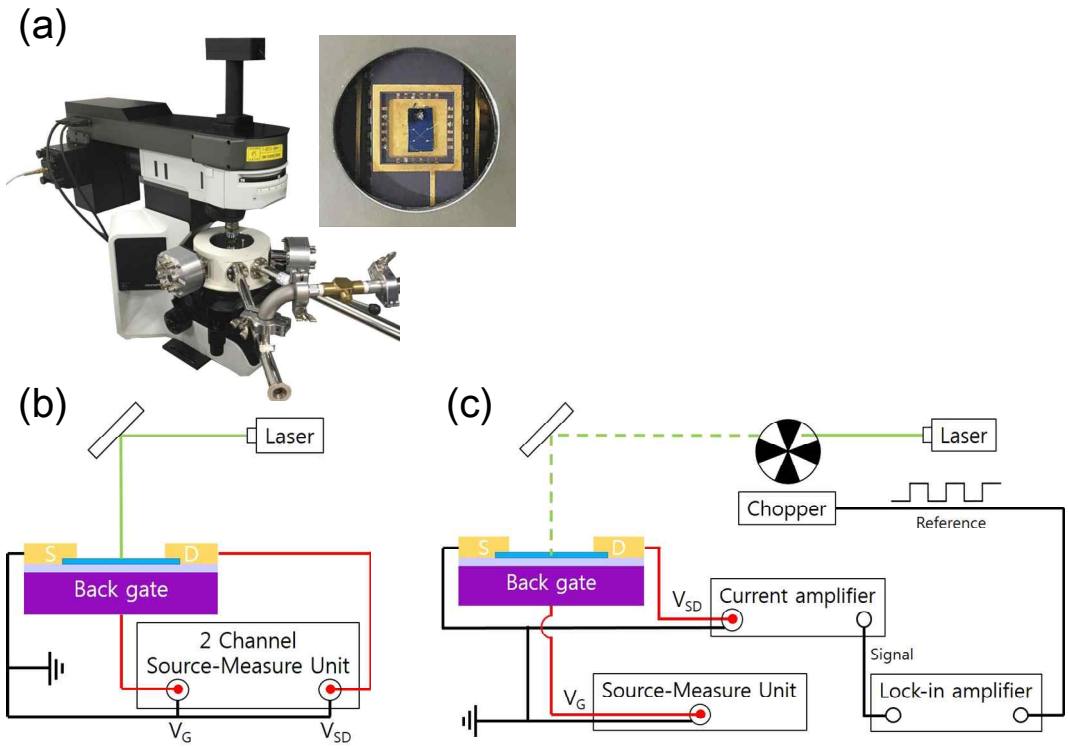

Figure S6. (a) Custom-made photocurrent scanning system mounted with a mini-cryostat. Schematic diagram of (b) DC and (c) AC photocurrent measurement setups. Inset is the optical image of our sample located inside the mini-cryostat.

5. Photoinduced gating (Photogating)

The effect of photoinduced gating on threshold voltage V_{th} is investigated for the devices with different substrates (SiO_2 and h-BN). For this study, the $J_{ds\text{-}pg}$–V_{gs} curves of each device were measured as a function of power and irradiation time, as shown in Fig. S7. To characterize the photogating effect, a DC measurement is conducted. This is shown in Fig. S6(b). Semilogarithmic plots of $J_{ds\text{-}pg}$–V_{gs} are drawn to manifest the photogating effect, since liner plots of $J_{ds\text{-}pg}$–V_{gs} do not clearly distinguish variations in $J_{ds\text{-}pg}$ near V_{th}. A liner plot of $J_{ds\text{-}pg}$–V_{gs} is shown in Fig. S7(e), with a linear extrapolation for the fit of V_{th}.

For the device on SiO_2 substrate, we first measure $J_{ds\text{-}pg}$–V_{gs} with zero optical intensity. This is marked as “before illumination” in Fig. S7(a). Then, $J_{ds\text{-}pg}$–V_{gs} is measured under various

optical intensities in Fig. S7(a). J_{ds} shifts toward the negative voltage proportionally to the illumination power from 5 pW/μm^2 to 500 pW/μm^2. The effect of photoinduced gating on the device with the h-BN substrate is more severe, as shown in Fig. S7(b). Under a power density of 60 pW/μm^2, $J_{ds\text{-}pg}$ exceeds our sweep range such that no off-state is observed in Fig. S7(b). This is the result of a lower SBH of the MoS_2 FET on h-BN than on SiO_2 substrate, which is shown in Figs. S5(b) and S5(d). On the SiO_2 substrate, once photogating occurs, it takes approximately 2 days for V_{th} to return to the initial value probed before the illumination. Such temporal variations in $J_{ds\text{-}pg}$ and V_{th} are presented in Figs. S7(c) and 7(d).

In Fig. S7(c), variations in $J_{ds\text{-}pg}$–V_{gs} of the MoS_2 FET on the SiO_2 substrate are obtained before and after the device is exposed to the light. Our laser is shone on the device for 1 h. The laser power is 2.5 pW/μm^2. During the exposure, $J_{ds\text{-}pg}$–V_{gs} of the device is frequently characterized in order to examine changes in V_{th} that progressively shift toward the negative voltage until we turn off the laser. The change in V_{th} of the device during the experiment is shown in Fig. S7(d). The initial V_{th} of the device was 21 V, as shown in Fig. S7(e). During the illumination, it decreased to 15.75 V [Fig. S7(d)]. Immediately after turning off the laser, V_{th} recovered to some degree [Fig. S7(d)]. However, after the laser was off for 20 min, the recovery slowed [Fig. S7(d)].

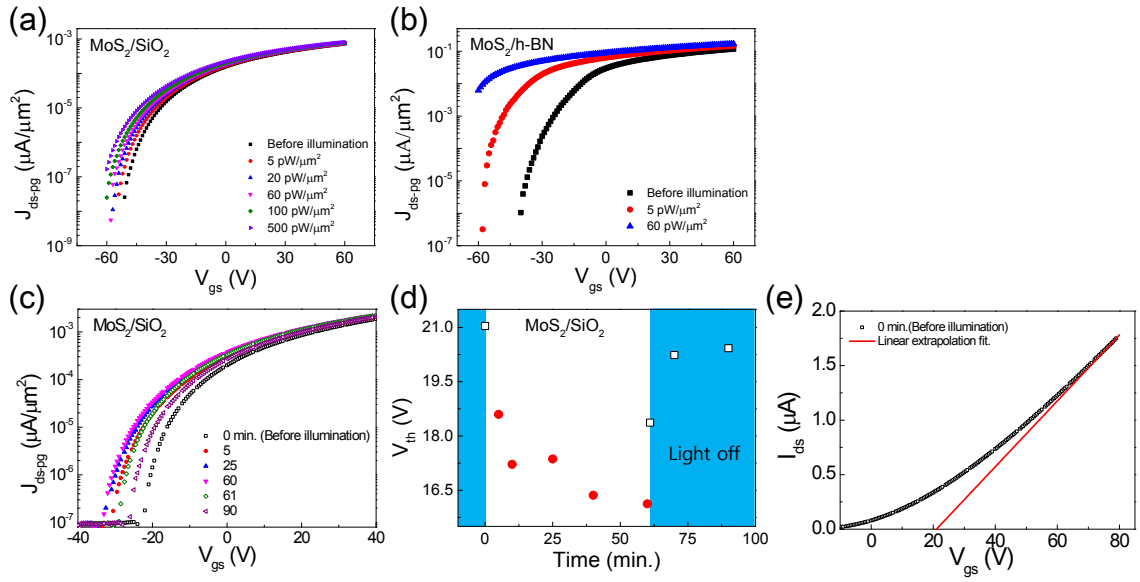

Figure S7. Shift of J_{ds} of MoS_2 FET on (a) SiO_2 and (b) h-BN substrates under various optical input powers. Temporal shifts of (c) J_{ds} and (d) of V_{th} of MoS_2 FET on SiO_2 substrate under optical input power of 2.5 pW/μm^2. (e) V_{th} of device tested in Figs. S7(c) and 7(d).

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