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Tight real-time synchronization of a microwave clock to an optical clock across a turbulent air path: supplementary material

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This document provides supplementary information to "Tight real-time synchronization of a microwave clock to an optical clock across a turbulent air path," http://dx.doi.org/10.1364/optica.3.000441. Here, we discuss details of the microwave clock and present a more detailed schematic.

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It is important to maintain tight phase coherence between the microwave oscillator and the local frequency comb that comprises the microwave clock. The setup is illustrated schematically in Fig. S1. The microwave oscillator is a combination of a quartz oscillator and a dielectric resonator oscillator (DRO). A quiet 100-MHz quartz oscillator is frequency multiplied by a factor of 100. The DRO is phase-locked to this 10-GHz signal with about 100-kHz bandwidth to reduce the phase noise level at high Fourier frequencies and for greater frequency flexibility. A self-referenced frequency comb is then phase-locked to this signal by mixing the 10.037-GHz output of the Quartz/DRO pair with the detected 50th harmonic of the comb's repetition frequency in a low-noise mixer to create a baseband phase error signal. The digital loop filter (implemented on a field-programmable gate array (FPGA)) that controls these actuators uses a 16-bit ADC to measure the phase error signal and its gains are adjusted to reach a 10-kHz lock bandwidth. Piezoelectric actuators close the feedback loop by changing the repetition frequency of the comb by adjusting the cavity length of the comb. With the feedback loop closed, there are three coherent outputs, one optical and two rf: the optical 200-MHz pulse train, the 10.037-GHz signal generated from direct photodetection of the frequency comb pulses, and the 10.037-GHz signal from the DRO.

With the system described above, the frequency comb is tightly locked to the microwave oscillator. To achieve synchronization, the system then adjusts the phase of the microwave oscillator as described next. First, the time offset is computed from the O-TWTFT master synchronization equation [1] by an FPGA-based controller co-located with the microwave clock. This time offset acts as an in-loop error signal that is filtered (as discussed in Section 3) and then used to adjust the frequency of the microwave oscillator. The frequency adjustment is implemented through an offset lock of the DRO to the 10-GHz quartz signal, as shown in Fig. S1. The offset is provided by an adjustable low-noise direct digital synthesizer (DDS) module. A 37 MHz nominal DDS frequency was used, leading to a 10.037-GHz DRO output.

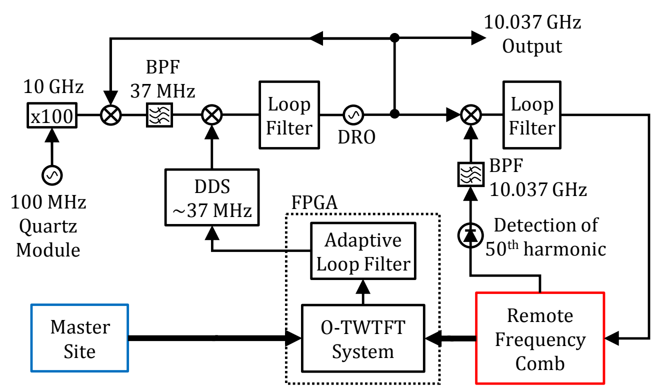

Fig. S1 Stabilization architecture for the microwave clock. BPF: bandpass filter, DRO: dielectric resonator oscillator, O-TWTFT: Optical two-way time-frequency transfer.

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