SUPPORTING INFORMATION

Low Variability in Synthetic Monolayer MoS_2 Devices

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A. Dry thermal SiO_2 on Si (p^{++}) Characterization

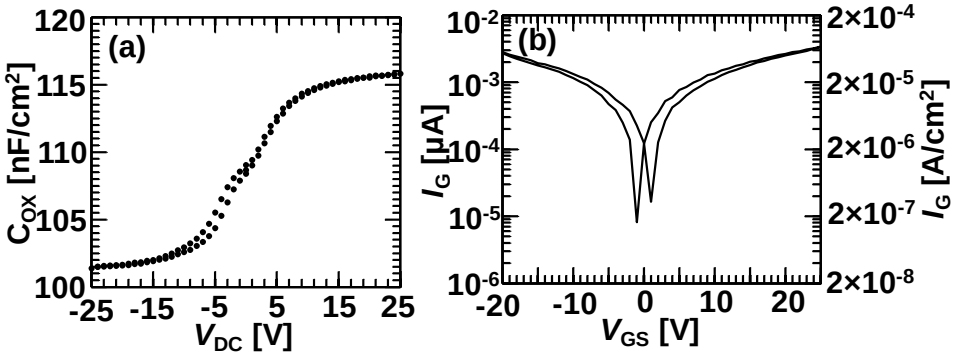

Figure S1. (a) Example C-V measurement (f = 100 kHz, v_{ac} = 30 mV) on a 40 nm Au/1 nm Ti/30 nm SiO_2/500 μm Si (p^{++}) MOScap, normalized to its area. The growing depletion capacitance in the p^{++} Si causes the <10% reduction in the measured capacitance for negative gate biases at this frequency. For V_{DC} > 15 V, the measured capacitance is above 115 nF/cm^2 and approaches the real value C_{ox} ~ 116 nF/cm^2. (b) Measured gate leakage for the same device shown in Figure 1f, both in absolute μA and normalized to the combined source and drain pad area of 5×10^3 μm^2 (also showing forward and backward sweeps). The total leakage remains well below 10^{-4} A/cm^2 for all V_{GS}, and is over four orders of magnitude below I_D at V_{GS} = 25 V. All our oxides are grown in-house at the Stanford Nanofabrication Facility (SNF) using a Thermco oxidation furnace and dry O_2 gas as the oxidant.

B. Process Flow for MoS_2 FET Fabrication and Measurement

All feature definition for this work was performed by optical photolithography using a KarlSuss MA-6 Contact Aligner system (365 nm, 15 mW/cm^2, hard contact mode with a 40 μm gap). For metallization steps, Shipley LOL 2000 was applied (60 s @ 3000 rpm) as a liftoff resist before application of SPR 3612 optical photoresist (PR). For the channel definition, only the latter was used. The two etch steps are done in a Materials Research Corporation model 55 reactive ion etcher (RIE), using 20 sccm O_2 at 10 W and a pressure of 20 mTorr. (We attribute the very small RMS surface roughness of our finished devices to this very gentle etch process.) All metallization steps

were performed in a Kurt J. Lesker electron beam metal evaporator at base pressures of ~5×10^{-8} Torr. (The low pressure of contact evaporation is crucial for good contacts.[S1]) Metal liftoff is done by soaking chips in MicroChem Remover PG at room temperature for at least one hour before spraying with acetone and methanol, and blow-drying with N_2.

The general process flow before measurement is as follows:

1. CVD synthesis of large-area MoS_2 nanofabrics on 30 nm SiO_2 on Si as detailed in Ref. S2.
2. Define probe pads in PR; etch MoS_2 in pad areas; deposit 2/40 nm Ti/Au; liftoff.
3. Define contact regions in PR; deposit 25/25 nm Ag/Au; liftoff.
4. Define channel regions in PR; etch exposed MoS_2; dissolve PR in acetone.
5. Mount chip in a Janis vacuum probe station, pump to pressure of ~2×10^{-5} Torr, and perform a two-hour *in-situ* vacuum anneal at 250 °C followed by an overnight cool-down period.
6. Measure devices *in-situ* at room temperature ~20 °C, in the same vacuum probe station.

C. Additional Statistical Data for V_{DS} = 1.0 V

Measured Quantity	Mean ⟨...⟩	Standard Deviation (s)	α for χ^2 test
Linear V_T	-1.78 V	1.05 V	0.02
Constant-current V_T	-7.42 V	1.79 V	0.46
$\sqrt{I_D}$ V_T	-7.06 V	2.17 V	10^{-5}
Y-function V_T	-0.51 V	0.99 V	0.37
Linear ΔV_T	0.16 V	0.12 V	10^{-3}
n_t	1.1×10^{11} cm^{-2}	0.9×10^{11} cm^{-2}	10^{-3}
$\log_{10}(H)$	-0.8885	0.2246	0.1
$\log_{10}(I_{MAX}/I_{MIN})$	6.6813	0.4015	10^{-7}
μ_{FE}	34.2 cm^2/V/s	3.6 cm^2/V/s	0.13
μ_Y	38.2 cm^2/V/s	4.4 cm^2/V/s	0.34
R_{CY}	3.0 kΩ·μm	0.7 kΩ·μm	10^{-4}
W	11.74 μm	0.13 μm	10^{-21}

Table S1. Means and standard deviations for all values extracted in this study at V_{DS} = 1.0 V. We recall that the V_T here is representative of the t_{ox} = 30 nm oxide thickness. Different equivalent oxide thickness (EOT) will rescale the V_T by the ratio EOT/t_{ox}.

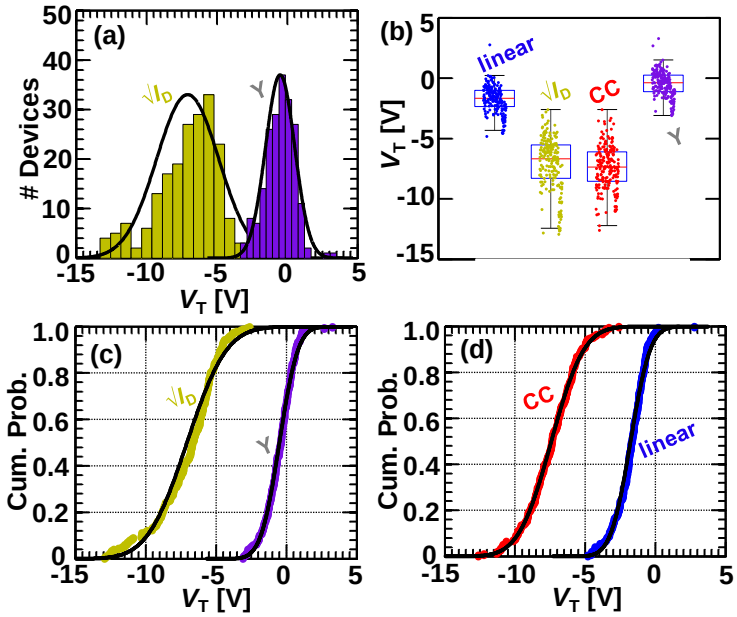

Figure S2. Statistical data representations for different V_T extractions. (a) Histograms and Gaussian fits of V_T extracted by the $\sqrt{I_D}$ (yellow) and Y-function (purple) methods. (b) Box-and-whisker plots of all four extractions, showing that standard deviations for the linear extrapolation and Y-function methods are smaller than those for $\sqrt{I_D}$ and constant-current. (c) Cumulative distribution function (CDF) plots of the same data in (a), with Gaussian fits (black lines). The goodness-of-fit is more easily visualized in this plot. (d) CDF plots of the data shown in Figure 2a.

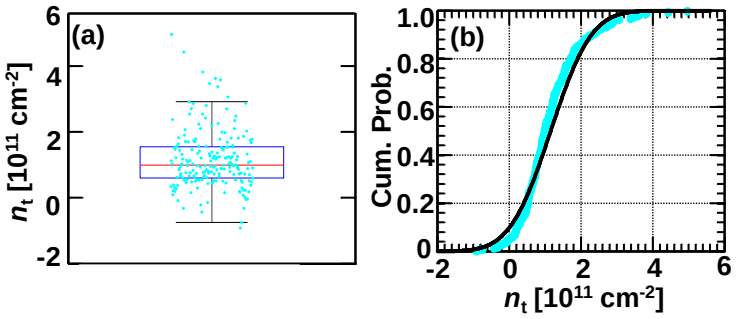

Figure S3. Additional representations of estimated density of charge traps n_t. (a) Box-and-whisker plot, and (b) CDF plot.

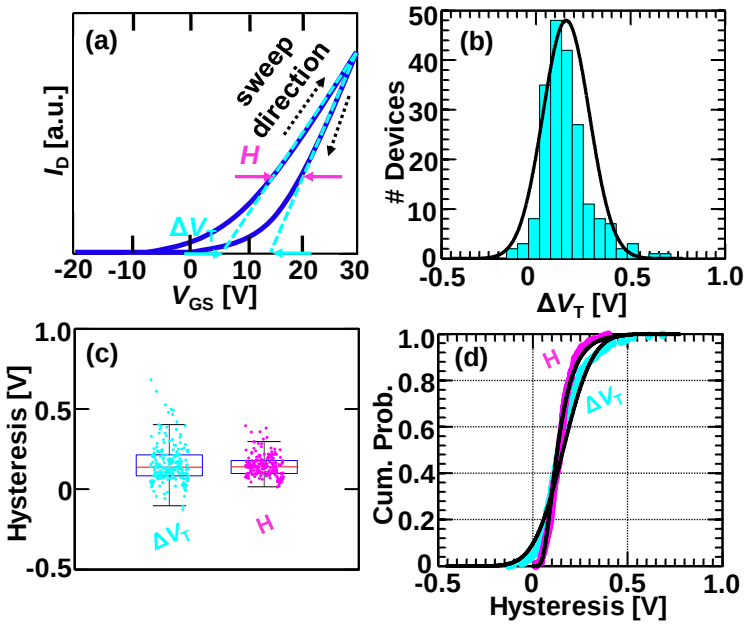

Figure S4. Additional representations of hysteresis extractions. (a) A mock-I_D-V_{GS} sweep with over-exaggerated hysteresis, showing how we extract ΔV_T and H. (b) ΔV_T as measured by linear extrapolation between the forward and backward I_D-V_{GS} sweep. These data correspond directly to Figure 2b of the main text by $n_t = \Delta V_T C_{ox}/q$. (c) Box-and-whisker plots of ΔV_T and the maximum measured hysteresis as taken between all points in the linear region of the forward and backward I_D-V_{GS} sweeps. Given the definitions in (a), it is unsurprising that typical values for H would be less than that for ΔV_T. (d) CDF plots of the same data in (c) along with Gaussian and lognormal fits (lines) for ΔV_T and H, respectively.

It should be pointed out that, despite all values for H being positive as expected, 5% of the extractions for ΔV_T are negative. This is an artifact of the extraction methodology combined with the fact that the hysteresis in our devices is indeed quite small. For any particular extraction of the forward and backward values for V_T, the 95% confidence intervals in the extraction (with the coefficient of determination $r^2 \geq 0.99999$) overlap by 95%. Loosely put, there is a 95% chance that the two values are the same, to 95% certainty in our measurement. This results in the error bars on either side of any one ΔV_T data point in Figures S4b-d being 20–25% greater than the mean value, which would ideally be zero. This highlights the importance of taking measurements on large numbers of data and running statistics. A more strict interpretation of the statistics will only lead to the conclusion that, in addition to ΔV_T being very small, we can only be 95% certain that the population mean $\mu_{\Delta VT}$ is indeed positive. Compare to Figure S11e, where all extractions for ΔV_T and n_t are positive.

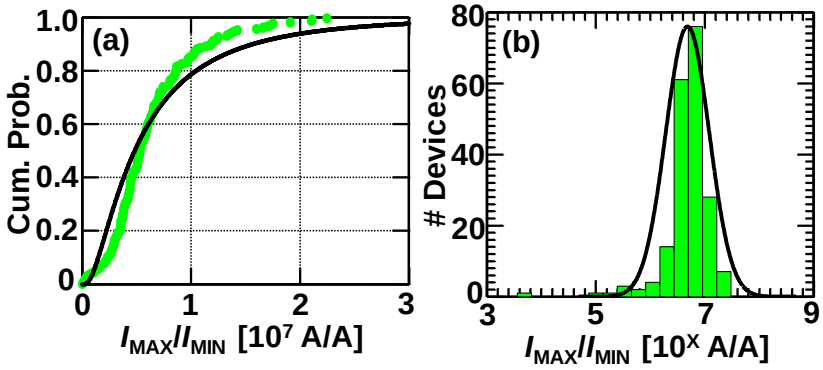

Figure S5. Additional representations of I_{max}/I_{min}. (a) CDF and (b) log-scale histogram plot. We choose the notation I_{max}/I_{min} instead of I_{on}/I_{off} because (1) this is simply the ratio of the highest to lowest measured current for each device, which could be different dependent upon V_T and measurement range of V_{GS}, and (2) on- and off-currents (I_{on}, I_{off}) are set by choosing voltage rails in e.g. a circuit, which we do not have here. Thus the term I_{on}/I_{off} is not well defined in this context.

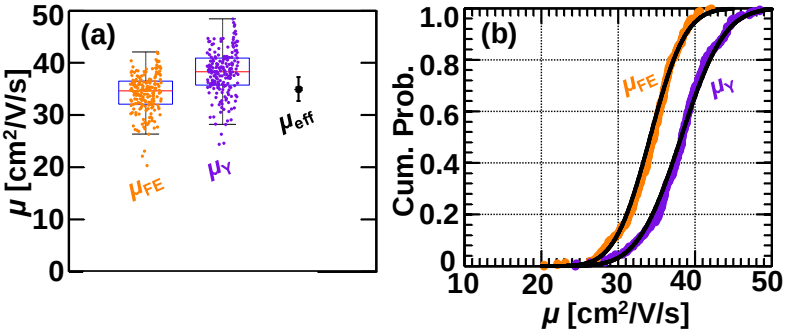

Figure S6. Additional representations of mobility extractions. (a) Box-and-whisker plot showing μ_{FE}, μ_Y, and μ_{eff} from the pTLM with 95% confidence intervals. (b) CDF plots for μ_{FE} (orange) and μ_Y (purple).

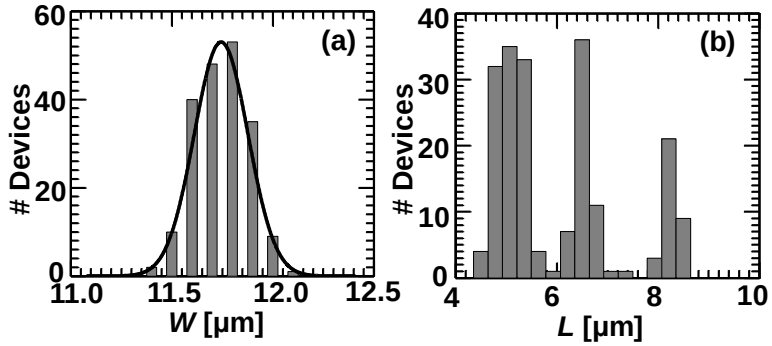

Figure S7. Histograms for geometry values as measured by SEM. (a) W is observed to be Gaussian with a standard deviation of 0.13 µm. (b) The histogram for device lengths L is trimodal since there were three nominal device lengths measured on the chip. Each distribution is itself Gaussian.

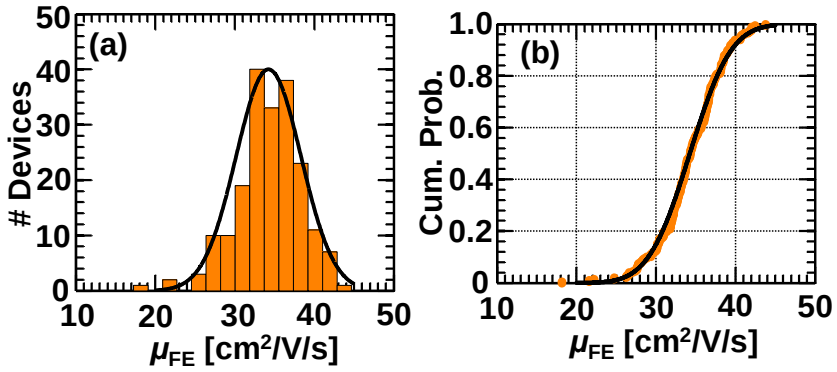

Figure S8. Extractions for μ_{FE} assuming that L and W are their mean values for each device. (a) While the mean is exactly the same, the variance of the histogram for μ_{FE} can be seen to increase slightly with this assumption. The coefficient of variation (CV) only increases slightly due to L and W having such small variances. (b) CDF plot of the data in (a), which may be contrasted to the orange data in Figure S6b.

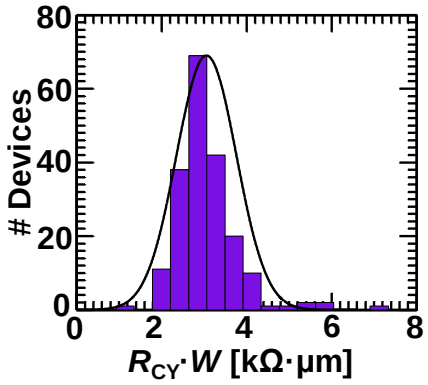

Figure S9. The histogram for R_{CY} shows a mean near 3.0 kΩ·μm.

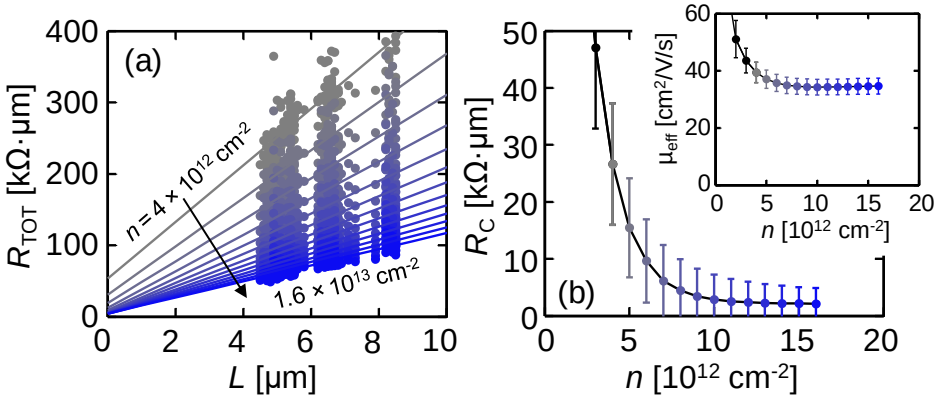

Figure S10. (a) pTLM analysis for V_{DS} = 1.0 V. (b) R_C = 2.1 ± 2.7 kΩ·μm at n = 1.6×10^{13} cm^{-2}. Inset: μ_{eff} = 34.7 ± 2.8 cm^2/V/s. Colors represent increasing carrier density.

D. Additional Statistical Data for V_{DS} = 0.1 V

Measured Quantity	Mean ⟨…⟩	Standard Deviation (s)	α for χ^2 test
Linear V_T	-2.36 V	1.08 V	0.04
Constant-current V_T	-2.06 V	1.56 V	0.02
$\sqrt{I_D}$ V_T	-7.61 V	2.10 V	10^{-3}
Y-function V_T	-1.13 V	1.10 V	0.16
Linear ΔV_T	0.29 V	0.09 V	10^{-4}
n_t	2.1×10^{11} cm^{-2}	0.6×10^{11} cm^{-2}	10^{-4}
$\log_{10}(H)$	-0.6745	0.1305	0.1
$\log_{10}(I_{max}/I_{min})$	5.8623	0.2513	10^{-4}
μ_{FE}	34.4 cm^2/V/s	3.9 cm^2/V/s	0.16
μ_Y	37.8 cm^2/V/s	4.7 cm^2/V/s	0.08
R_{CY}	2.9 kΩ·μm	0.9 kΩ·μm	10^{-7}

Table S2. Means and standard deviations for all values extracted in this study at V_{DS} = 0.1 V. Compare with Table S1 values extracted at V_{DS} = 1.0 V.

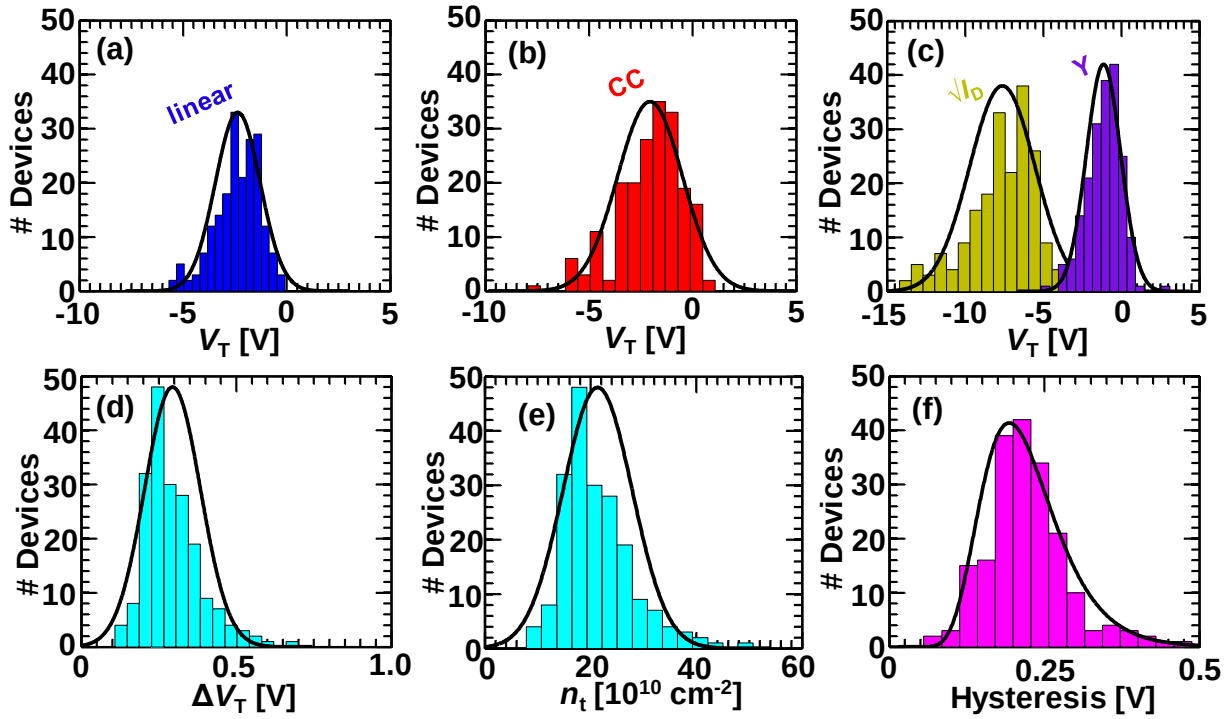

Figure S11. Statistical data representations for the different V_T extractions, ΔV_T, n_t, and H all for V_{DS} = 0.1 V. (a)–(c) Histograms and Gaussian fits of V_T as extracted by the four methods previously mentioned. (d) and (e) ΔV_T and n_t histograms, related by $n_t = \Delta V_T C_{ox}/q$. Note that all values of ΔV_T are positive in this case, as is generally expected. (f) Histogram of measured hysteresis H, which is again lognormal. All values are consistent with those extracted for V_{DS} = 1.0 V in Figure 2.

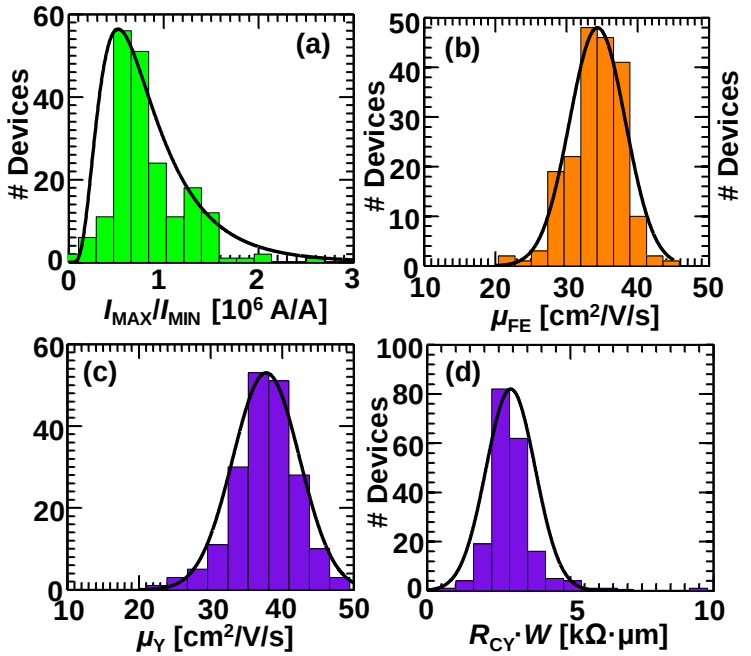

Figure S12. Histograms for V_{DS} = 0.1 V. (a) Histograms and lognormal fit of I_{max}/I_{min}. Note that these values have fallen by approximately one order of magnitude compared to V_{DS} = 1.0 V (see Figure 2d in main text), since these devices are operating in triode and contact resistance is relatively small. (b) μ_{FE} values are again the same as for V_{DS} = 1.0 V (Figure 2e). (c) and (d), mobility and contact resistance as extracted from the Y-function method (compare to Figure 2f at V_{DS} = 1.0 V).

E. Extractions Using the Y-Function Method

As expounded in Ref. S3, mobility can be estimated from the Y-function, $Y = I_D / \sqrt{g_m}$, by the expression $\mu_Y = \left(\frac{Y}{V_{GS} - V_T}\right)^2 \left(\frac{L}{WC_{ox}V_{DS}}\right)$, where V_T is estimated by linear extrapolation from a plot of Y vs. V_{GS} rather than I_D vs. V_{GS}. Further, an upper bound on the minimum single-contact resistance in the strong inversion regime can be estimated by $R_{CY}W \approx \frac{\theta L}{2C_{ox}\mu_Y}$, where θ is a V_{GS}-dependent attenuation factor with units of V^{-1} in the expression $I_D = \frac{\mu_Y}{1+\theta(V_{GS}-V_T)} C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS}$. From these equations, we calculate μ_Y = 38.2 ± 8.8 cm²/V/s and $R_{CY}W$ = 3.0 ± 1.4 kΩ·μm for V_{DS} = 1.0 V.

F. International Technology Roadmap (ITRS) specifications

In simulations, we optimize the flat band voltage of the top gate (V_{FB}) for each channel length such that the I_{off} (at V_{GS} = 0, V_{DS} = V_{DD}) = 100 nA/μm. Other device parameters used are as per ITRS[S4] specifications as shown in the table below.

L (nm)	t_{ox} (nm)	V_{DD} (V)	R_C (Ω·μm)
16	0.8	0.86	188
32	1.1	1.1	180
65	1.3	1.2	190
500	5.0	3.3	200

Table S3. The device parameters used to simulate MoS_2 transistors with ITRS specifications.[S4]

G. Monte Carlo simulations of standard cells

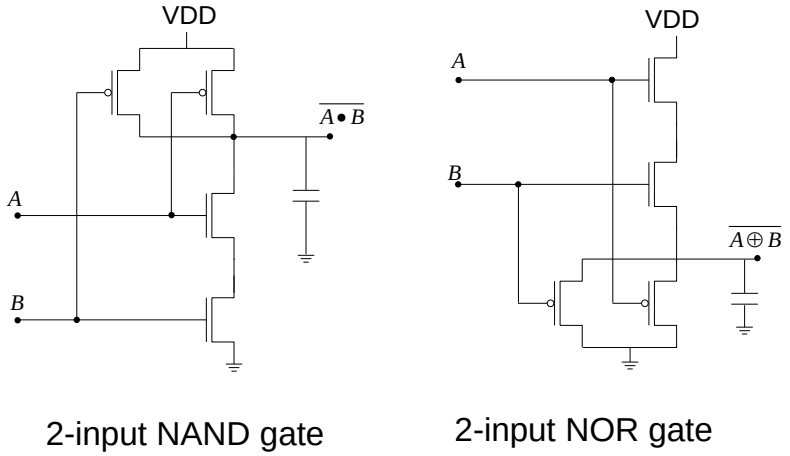

Figure S13. Schematic for 2-input NAND and NOR gate

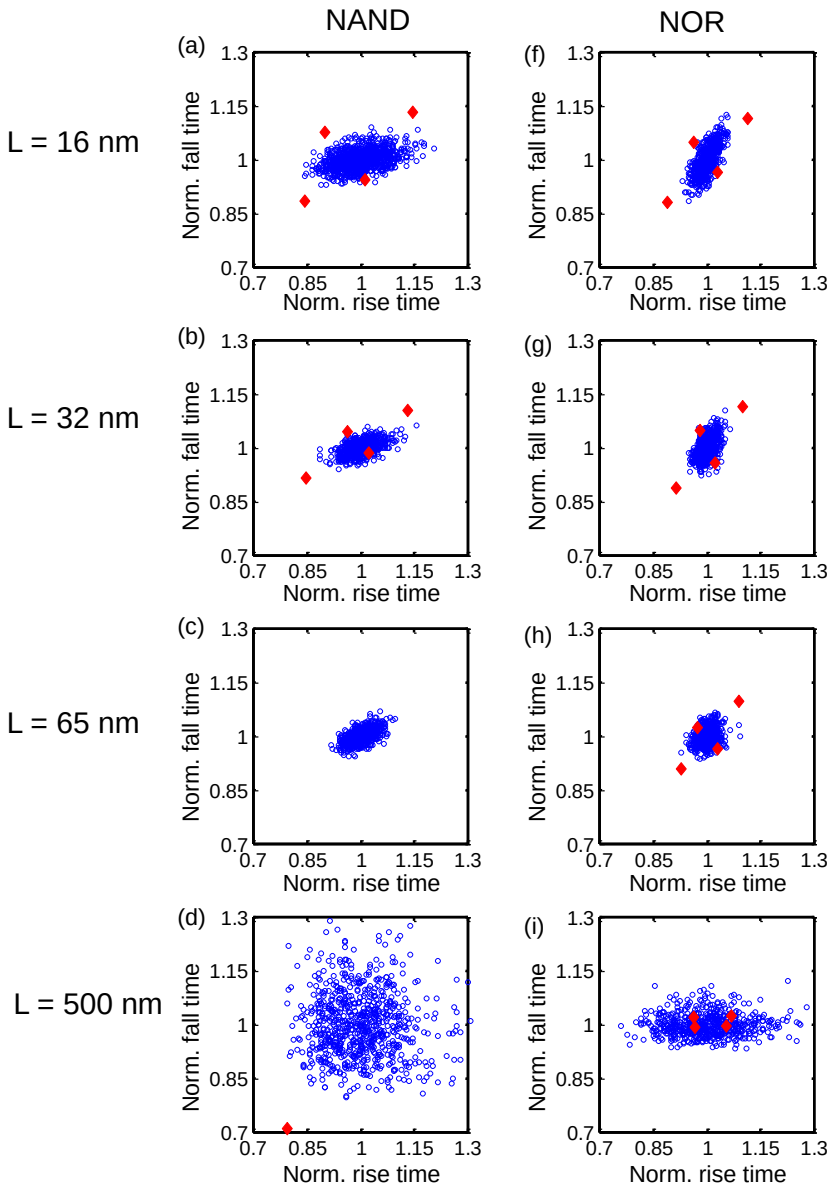

Figure S14. (a) to (f) show Monte Carlo simulations of fall time (τ_{Fall}) and rise time (τ_{Rise}) of NOR2 for 16 nm and 65 nm technology nodes respectively. We have normalized the rise time and fall time for each channel length with respective mean values. The performance corners [NFET-PFET: Fast-Fast (FF), Slow-Slow (SS), Fast-Slow (FS) and Slow-Fast (SF)] are calculated for $\langle \mu_{\text{FE}} \rangle \pm 2s_{\mu\text{FE}}$. The simulated values for the performance corners are shown in red diamonds.

Supplementary References

(S1) English, C. D.; Shine, G.; Dorgan, V. E.; Saraswat, K. C.; Pop, E. Improved Contacts to MoS_2 Field-Effect Transistors by Ultra-High Vacuum Metal Deposition. *Nano Lett.* **2016**, *16*, 3824–3830.

(S2) Smithe, K. K. H.; English, C. D.; Suryavanshi, S. V; Pop, E. Intrinsic Electrical Transport and Performance Projections of Synthetic Monolayer MoS_2 Devices. *2D Mater.* **2017**, *4*, 011009.

(S3) Chang, H.-Y.; Zhu, W.; Akinwande, D. On the Mobility and Contact Resistance Evaluation for Transistors Based on MoS_2 or Two-Dimensional Semiconducting Atomic Crystals. *Appl. Phys. Lett.* **2014**, *104*, 113504.

(S4) International Technology Roadmap for Semiconductors (ITRS). High Performance (HP) and Low Power (LP) PIDS Tables. URL: <http://www.itrs2.net/itrs-reports.html>.