Supporting Information

Variability Improvement of TiO_x/Al₂O₃ Bi-layer Nonvolatile Resistive Switching Devices by Interfacial Band Engineering with Ultra-thin Al₂O₃ Dielectric Material

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Figure S1. Initial forming voltage distribution with different TiO_x/Al_2O_3 RRAM devices. Device-to-device forming voltage distribution for (a) S1, (b) S2, and (c) S3 devices. Due to the thicker Al_2O_3 layer, the S1 devices need higher voltage as compare to the S3 devices.



Figure S2. Transition from HRS to LRS in S1 RRAM devices. The cycle-to-cycle transition from HRS to LRS is showing a non-uniform evolution of CNF. Due to that the variation in resistive switching cycles are obvious.



Figure S3. Variation of LRS and HRS. The cycle-to-cycle variation of the LRS for (a) S1, (b) S2, and (c) S3 devices, respectively. The cycle-to-cycle variation of the HRS for (d) S1, (e) S2, and (f) S3 devices, respectively. In all cases the controllability is improving the 2 nm Al_2O_3 based RRAM device structure.



Figure S4. Surface plot of variation. The surface plot of variation is showing an excellent control of the variability by ultra-thin 2 nm Al_2O_3 layer as compare to the thicker Al_2O_3 layer.



Figure S5. The LRS conduction. (a) The TAT conduction is dominating at the lower voltage and (b) the F-N tunneling conduction is dominating at the higher voltage for S1 RRAM devices with 8 nm thick Al_2O_3 layer. (c) The high *E* can modify the tunnel barrier thickness < 2.5 nm and the conduction is by F-N tunneling. But with lowering the *E* the height of the triangular potential barrier is increasing, resulting an increasing thickness for the electron tunneling. In this situation TAT is dominating. (d) For an ultra-thin 2 nm Al_2O_3 based S3 RRAM devices, the F-N tunneling is controlling the conduction over a large voltage range.